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Work function characterization of solution-processed cobalt silicide

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Abstract
Cobalt silicide thin films were prepared by spin-coating liquid cyclohexasilane-based inks onto silicon substrates followed by a thermal treatment. The work function of the solution-processed Co–Si was determined by both capacitance–voltage (C–V) measurements of metal–oxide–semiconductor (MOS) structures as well as by ultraviolet photoemission spectroscopy (UPS). Variable frequency C–V of MOS structures with silicon oxide layers of variable thickness showed that solution-processed metal silicide films exhibit a work function of 4.36 eV with one Co–Si film on Si ⟨100⟩ giving a UPS-derived work function of 4.80 eV. Similar work function measurements were collected for vapor-deposited MOS capacitors where Al thin films were prepared according to standard class 100 cleanroom handling techniques. In both instances, the work function values established by the electrical measurements were lower than those measured by UPS and this difference appears to be a consequence of parasitic series resistance.

1. Introduction
Metal silicide thin films are integral parts of microelectronic devices having been used as ohmic contacts, Schottky barrier contacts, gate electrodes, local interconnects and diffusion barriers [1]. Circuits comprised of silicon nanowires (Si NWs) are being considered for next generation integrated circuits and the development of ohmic contacts is a challenging and relevant part of the equation [2]. Cobalt silicide forms a stable, ohmic contact to silicon where thin films are typically formed by depositing cobalt metal onto a silicon wafer with the highly conducting CoSi2 phase forming during thermal treatment at moderate temperature (700 °C). The transformation of the Co/Si structure to CoSi2 gives an ohmic contact but necessarily requires consumption of the base silicon substrate at a ratio of 1 nm Co metal consuming 3.6 nm of Si [3]. Unfortunately, this phenomenon could minimize the utility of metal silicide contacts in future applications that utilize Si NWs in field-effect transistors [4–7] and non-volatile memory [8]. Indeed, high-resolution electron microscopy showed that attempts to produce a TiSi2 ohmic contact to Si NWs resulted in contact failure owing to voids that form as a consequence of silicon out-diffusion [2] (i.e. the Kirkendall effect) [9].

We have recently developed solution routes to silicon-based electronic materials using cyclohexasilane (Si6H12 or CHS) [10, 11] and have found that the addition of an appropriate cobalt reagent gives a viscous liquid that may be used in the solution synthesis of Co–Si phases in thin film form. This approach offers the possibility for metal silicide contacts to Si NWs whereby void formation is obviated as the Si6H12 provides a source of silicon rather than the Si NW substrate. In this paper, we report on the work function (Φm) of metallic cobalt silicide films prepared from a cobalt-containing Si6H12-based ink as determined by C–V analysis of curves of metal–oxide–semiconductor (MOS) structures and directly by ultraviolet photoemission spectroscopy (UPS).

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2. Experimental details

Si₆H₁₂ was prepared according to a previous report [12] and distilled under reduced vacuum yielding 99+% pure colorless liquid (by ¹H nmr). Inert atmosphere gloveboxes and standard Schlenk techniques were used to preclude the oxidation of liquid silanes. (Note: Si₆H₁₂ and the cobalt–silane mixtures are pyrophoric liquids that burn upon contact with air and even small quantities should be treated as an ignition source and handled with care under inert atmosphere.) A liquid precursor containing cobalt and silicon was prepared by dissolving Co₂(CO)₈ (2.65 g, 7.5 mmol) in 20 mL CH₂Cl₂ in a 100 mL round bottle flask and adding Si₆H₁₂ (0.90 g, 5.0 mmol) with a pipette over a 3 min period. The evolution of gas was noted as bubbles during initial addition. After stirring at room temperature for 24 h, the solvent was removed under vacuum to give a dark red–brown viscous liquid (~2.1 g). Dry, sparged toluene was then added to the viscous liquid in an approximate 1:9 ratio giving the Co–Si ink.

B-doped p-type (100) Si 101 mm diameter wafers 500 ± 25 μm thick with a 300 ± 21 nm SiO₂ layer were procured from University Wafer (lot B826301) and etched with buffered HF to achieve various gate oxide thicknesses (measured using a Nanometrics Nanospec reflectometer). Four-point probe measurements were performed using a Microtech CPS probestation (osmium probes with radii of 0.05 mm and a spacing of 1.0 mm) connected to a Keithley 2400 sourcemeter. Ten resistance measurements on one wafer gave a value of 58 ± 8 Ω which correlates to a sheet resistance of 264 Ω/square. A real resistivity of 5.3 Ω cm is derived when using wafer thickness of 0.5 mm and a correction factor of 0.4. This resistivity value gives an acceptor concentration of 2.6 × 10¹⁵ cm⁻³ as observed in a standard table (see, for example, www.pveducation.org/calc/resistivity).

Co–Si thin films were prepared by spin coating the Co–Si ink onto the SiO₂/Si wafer samples at 3000 rpm for 30 s giving the MOS test structures. Figure 1 shows the generic test structure for the MOS capacitors. The precursor film was thermally transformed into Co–Si via rapid thermal annealing at 700 ± 5°C for 60 s under N₂. Grazing incidence x-ray diffraction (GIXRD) characterization of the Co–Si thin films showed no reflections in spite of a metallic luster. A mixture of CoSi and CoSi₂ was observed by GIXRD for similarly processed Co–Si films with unambiguous phase identification after thermal treatment at 1100 °C (figure S1, available from stacks.iop.org/SST/27/000000/mmedia). The Co–Si films were patterned into 0.5 × 0.5 mm² squares using photolithography and reactive ion etching with CF₄/Ar plasma (70 sccm : 30 sccm) at 100 W rf power and 50 mbar pressure [13]. An Agilent B1500A semiconductor analyzer was calibrated to correct for phase error, stray admittance and residual impedance and then used to measure C–V with a 50 mV peak-to-peak ac signal from 1 kHz to 5 MHz and dc sweep from −5 to 3 V. A total of 58 Co–Si MOS capacitors with different gate oxide thickness were measured. Direct work function measurements were made by comparing the secondary photoemission cutoff of the unknown sample against freshly evaporated films of gold and silver with work functions of 5.1 and 4.7 eV [14]. The secondary photoelectrons were created with a helium lamp (He I emission at hv = 21.2 eV) and analyzed with a Kratos Axis HS hemispherical electron energy analyzer.

3. Results and discussion

Φₚ of the gate metal of a MOS capacitor can be estimated using equation (1) where most terms are a function of the material characteristics of the semiconducting silicon wafer (i.e. band gap energy E_g = 1.12 eV, electron affinity χ_Si = 4.05 eV, intrinsic carrier concentration n_i = 1.02 × 10¹⁰ cm⁻³, and doping concentration N_a = 2.6 × 10¹⁵ cm⁻³) [15]. Experimental values for metal-to-semiconductor work function difference, Φ_m (in eV), can be determined by plotting flat band voltage (V_{FB}) as a function of effective oxide thickness (EOT_{ox}) as described below.

Φ_m = Φ_m + χ_Si + 0.5E_g + kT ln \left( \frac{N_a}{n_i} \right).

(1)
The EOT_{ox} values from C–V measurements varied only slightly (i.e. 0–12%) from those measured by ellipsometry which suggests little interdiffusion between Co–Si and the SiO₂ underlayer and is consistent with previous data for Co films on SiO₂ where CoO decomposes to Co after 30 s at 700 °C [16]. C–V measurements of several Co–Si MOS structures that maintained variable EOT_{ox} were collected at 1 kHz (figure 2). A constant C is noted for gate voltage (V_g) less than −4 V where the majority carriers in the p-type semiconductor silicon wafer (i.e. holes) are accumulated at the Si/SiO₂ interface with the device acting as a parallel plate capacitor [17]. A depletion of the majority carriers is noted for V_g from −1 to 0 V where the capacitance drops as the depletion region expands with the outflow of majority carriers. Forward bias of the gate gives an inversion in the type of surface conductivity where the minority carriers now dominate the Si/SiO₂ interface [17]. Frequency-dependent C–V (figure 3) of the Co–Si MOS capacitors shows that samples probed at higher frequencies exhibit lower capacitance as anticipated. C–V data for Al MOS structures at variable gate oxide thickness (figure 4) and frequency (figure 5) show similar trends. The dispersion of the frequency-dependent C–V data appears to be related to the parasitic effect of series resistance (see below).

For the devices fabricated in this study, the capacitance of MOS capacitors at strong accumulation is inversely proportional to frequency (C \propto 1/f) and is also dependent on EOT_{ox} as C = \varepsilon_{0}/C_{ox} where \varepsilon_{0} is permittivity of vacuum, \varepsilon_{ox} is relative permittivity of SiO₂ (i.e. 3.9) and A is the gate area. In the idealized case, the C–V characteristics of MOS capacitors are frequency independent and the accumulation region capacitance remains constant irrespective of frequency [18]. However, lossy dielectric layers present at the oxide/semiconductor interface are known to cause frequency-dependent capacitance in the strong accumulation region [19]. The C–V characteristics of Co–Si MOS capacitor exhibit such departure from ideality.

The accumulation region for MOS capacitors can be modeled as a series combination of a capacitor C_{ox} representing the thermal oxide capacitance, and a resistor R_s subscripting substrate resistance (as a prime contributor) as well as the back contact and cable resistances. R_s can be readily extracted from the G–V and C–V curves of MOS capacitors using equation (2) from [21] where C_{ox} and G_{ox} represent the measured capacitance and conductance in strong accumulation region and \omega is the measurement frequency.

\[ R_s = \frac{G_{ox}}{(C_{ox})^2 + (\omega C_{ox})^2}. \]  

The equivalent capacitance (C_{eq}) of C_{ox} and R_s combination can be extracted according to equation (3) from [21]. At lower frequency, \omega \ll 1 hence C_{eq} \approx C_{ox}. At higher frequency, R_s decreases and \omega increases making R_s \omega^2 > 1 which leads to C_{eq} < C_{ox}. Hence the equivalent capacitance measured during accumulation would be smaller at higher frequencies. This phenomenon is common in metal–insulator–semiconductor (MIS) capacitors [22] and reasonably aligns with the measured R_s data for these Co–Si MOS capacitors (figure S2, available from...
measured to be 0.389 eV which represents an error of the work function of Au (5.10 eV) and Ag (4.73 eV) was estimated from EOTox versus VFB data for an Al-based MOS capacitor with gate oxide thickness ranging from 22 to 240 nm.

The extrinsic Debye length (λ) is a measure of the distance over which a charge imbalance in a MOS capacitor is neutralized by majority carriers under equilibrium [23]. An extrinsic Debye length of 8.01 × 10^{-8} m was calculated according to equation (4) where \( \varepsilon_{\text{sub}} = 11.68 \) relative permittivity of p-type Si, \( k = 1.38 \times 10^{-23} \) JK^{-1} Boltzmann constant, \( T = 300 \) K and \( N_a = 2.6 \times 10^{15} \) cm^{-2}. The flat band capacitance (Cfb) of the MOS structure is determined according to equation (5) [24].

\[
\lambda = \sqrt{\frac{\varepsilon_{\text{sub}} \varepsilon_0 k T}{q^2 N_a}} \tag{4}
\]

\[
C_{\text{fb}} = \frac{C_{\text{ox}}}{C_{\text{ox}} \left( \varepsilon_{\text{sub}} \times \frac{4}{2} \right)} \tag{5}
\]

Cfb values calculated using equation (5) were located on each of the C–V data curves in figure 7. Linear interpolation of these points to the x-axis defines the flat band voltage, VFB, for each of the various EOTox curves [25, 26]. The \( \Phi_{\text{ms}} \) for the MOS structures is defined as the y-axis intercept of the line estimated from EOTox versus VFB data [15]. A value of \(-0.575\) for \( \Phi_{\text{ms}} \) was thus determined for Co–Si MOS capacitors (figure 7) which plugs into equation (1) to give a C–V-derived \( \Phi_m \) of 4.36 eV for the solution-processed Co–Si. Similar analysis of the EOTox versus VFB data for Al MOS capacitors (figure 8) gives \( \Phi_{\text{ms}} \) of \(-0.451\) which equates to a \( \Phi_m \) of 4.48 eV for sputtered Al.

To independently and directly determine the work function of solution-processed Co–Si materials, a thermally-treated Co–Si film on a 1 x 1 cm² Si wafer substrate (<0.005 Ω cm) was analyzed by UPS. Additionally, an Al thin film on a 1 x 1 cm² Si wafer substrate (<0.005Ω cm) was also measured. The difference between the work function of Au (5.10 eV) and Ag (4.73 eV) was measured to be 0.389 eV which represents an error of \( \sim 5% \) for the method. UPS analysis of a Co–Si film on a conducting Si wafer gave a \( \Phi_{\text{ms}} \) value of 4.80 eV (figure 9) which is near that previously reported for a CoSi2 film prepared by heating a Co film on Si (i.e. \( \Phi_m = 4.77 \) eV) [27]. A work function of 4.40 eV was derived for the Al film (figure 9) which compares favorably to literature (i.e. \( \Phi_m = 4.28 \) eV) [28].

The \( \sim 0.4 \) eV difference between UPS- and C–V-based \( \Phi_m \) for the solution-processed Co–Si thin films can be explained by interface trapped charges (Qu) [17]. Such traps might arise as a consequence of defects in the thermal SiO2 layer or perhaps from Li⁺ impurities in the Co–Si layer given residual LiCl during the LiAlH4 reduction step in the synthesis of Si6H12 [12]. MOSCap software [29] was used to simulate how the C–V curve shifts as a consequence of \( Q_u \). All the simulation parameters mimicked those used in the experiment with \( \Phi_m \) set to 4.80 eV and a gate silicon oxide thickness of 113.6 nm. The MOSCap results along with experimental data for a solution-processed Co–Si MOS capacitor are plotted in terms of capacitance versus gate voltage in figure 10. Simulation of a Co–Si MOS capacitor with an ideal interface (\( Q_u = 0 \)) shows the transition to depletion at higher Vg versus the solution-processed sample. The inclusion of interface charge traps in the MOSCap program causes the...
PMOS devices require \( \Phi_1 \) appears to be a candidate for gate electrodes where NMOS and from Si 6H12 inks and metal silicide source channel length 10–20 of all-solution-processed transistors on the mesoscale (i.e. NWs, an intermediate goal for this work is the development capacitors.
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Acknowledgments

4. Conclusions

We have prepared Co–Si thin films using a solution process. The \( C-V \) and UPS-derived \( \Phi_m \) (i.e. 4.36 and 4.80 eV, respectively) for Co–Si are close to common metals used in microelectronics such as Ti (4.33 eV) [28], Ag (4.26 eV) [28] and Al (4.28 eV) [28]. Therefore, solution-processed Co–Si appears to be a candidate for gate electrodes where NMOS and PMOS devices require \( \Phi_m \) near 4.1 and 5.2 eV, respectively [30]. Prior to developing this process at the nanoscale for Si NWs, an intermediate goal for this work is the development of all-solution-processed transistors on the mesoscale (i.e. channel length 10–20 \( \mu \)m) that comprise poly-Si channels from Si\(_6\)H\(_{12}\) inks and metal silicide source/drain contacts from Co–Si inks. While the present study shows that solution-processed Co–Si has good interface stability with both thermal SiO\(_2\) and Si wafer, grain boundaries will be an additional consideration when using poly-Si instead of wafer Si. An additional complexity is the stepwise thermolysis known for cyclohexasilane (i.e. Si\(_6\)H\(_{12}\) \( \rightarrow \) polydiydrosilane \((\text{SiH}_2)_n\r) \rightarrow \text{a-Si:H} \rightarrow \text{poly-Si}) where the nature of Co–Si source and drain contacts to the channel contacts will depend upon the thermal history of the Si\(_6\)H\(_{12}\)-derived poly-Si film prior to solution deposition of the Co–Si ink.

References

[8] Zhu X X et al 2011 Nanotechnology 22 254020
[20] Iniewski K et al 1989 Solid-State Electron. 32 137–40
[24] Bentarzi H 2011 Transport in Metal-Oxide-Semiconductor Structures (Berlin: Springer)